

United States Patent and Trademark Office

UNITED STATES DEPARTMENT OF COMMERCE United States Patent and Trademark Office Address: COMMISSIONER FOR PATENTS P.O. Box 1450 Alexandria, Virginia 22313-1450 www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/046,597	12/18/2001	Gilbert Yoh	10011042-1	2843
7	590 04/12/2005		EXAM	INER
AGILENT TECHNOLOGIES, INC.			WARE, CICELY Q	
Legal Departm	ent, DL429			
Intellectual Property Administration		ART UNIT	PAPER NUMBER	
P.O. Box 7599			2634	
Loveland, CO	80537-0599		DATE MAILED: 04/12/2009	5

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)				
0.00	10/046,597	YOH ET AL.				
Office Action Summary	Examiner	Art Unit				
	Cicely Ware	2634				
The MAILING DATE of this communication Period for Reply	appears on the cover sheet v	vith the correspondence addre	∌SS			
A SHORTENED STATUTORY PERIOD FOR RE THE MAILING DATE OF THIS COMMUNICATIO - Extensions of time may be available under the provisions of 37 CFR after SIX (6) MONTHS from the mailing date of this communication. - If the period for reply specified above is less than thirty (30) days, a - If NO period for reply is specified above, the maximum statutory per - Failure to reply within the set or extended period for reply will, by state Any reply received by the Office later than three months after the meanned patent term adjustment. See 37 CFR 1.704(b).	N. R 1.136(a). In no event, however, may a reply within the statutory minimum of the riod will apply and will expire SIX (6) MC atute, cause the application to become a	a reply be timely filed hirty (30) days will be considered timely. DNTHS from the mailing date of this comm ABANDONED (35 U.S.C. § 133).	nunication.			
Status						
1) Responsive to communication(s) filed on 18						
·—	 This action is FINAL. 2b) This action is non-final. Since this application is in condition for allowance except for formal matters, prosecution as to the merits is 					
	closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.					
Disposition of Claims						
4) Claim(s) 1-20 is/are pending in the applicate 4a) Of the above claim(s) is/are without 5) Claim(s) 8-20 is/are allowed. 6) Claim(s) 1-5 is/are rejected. 7) Claim(s) 6 and 7 is/are objected to. 8) Claim(s) are subject to restriction and	drawn from consideration.					
Application Papers						
9)☑ The specification is objected to by the Exam 10)☑ The drawing(s) filed on 18 December 2001 is Applicant may not request that any objection to the Replacement drawing sheet(s) including the containing the oath or declaration is objected to by the	is/are: a)⊠ accepted or b)[the drawing(s) be held in abeya rection is required if the drawin	ance. See 37 CFR 1.85(a). g(s) is objected to. See 37 CFR	1.121(d).			
Priority under 35 U.S.C. § 119						
12) Acknowledgment is made of a claim for fore a) All b) Some * c) None of: 1. Certified copies of the priority documents. 2. Certified copies of the priority documents. 3. Copies of the certified copies of the priority documents. * See the attached detailed Office action for a	ents have been received. ents have been received in priority documents have bee reau (PCT Rule 17.2(a)).	Application No n received in this National St	age			
Attachment(s)						
 Notice of References Cited (PTO-892) Notice of Draftsperson's Patent Drawing Review (PTO-948) 		Summary (PTO-413) o(s)/Mail Date				
Notice of Draitsperson's Patent Drawing Review (PTO-946) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/Paper No(s)/Mail Date		Informal Patent Application (PTO-1	52)			

Art Unit: 2634

DETAILED ACTION

Specification

1. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

- 2. Claim 2 is objected to because of the following informalities:
- a. Claim 2, line 3, applicant uses "incracsing". Examiner suggests using "increasing" for clarification purposes.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

- 3. Claims 4, 10 and 17 recites the limitation "the group consisting".
- a. Claim 4, line 2, recites the limitation "the group consisting". There is insufficient antecedent basis for this limitation in the claim.
- b. Claim 10, line 2, recites the limitation "the group consisting". There is insufficient antecedent basis for this limitation in the claim.
- c. Claim 17, line 2, recites the limitation "the group consisting". There is insufficient antecedent basis for this limitation in the claim.

Art Unit: 2634

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

- (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 5. Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fong et al. (US Patent Application 2002/0154718), in view of Masleid et al. (US Patent 6,532,544).
- (1) With regard to claim 1, Fong et al. discloses in (Fig. 1 and Fig. 2) a system for matching data and clock signal delays, comprising: a clock buffer (Fig. 2 (105)) for driving said received clock signal to a register; a data receiver (Fig. 2 (115)) for removing noise from received data (Pg. 1, lines 31-43, 46-47).

However Fong et al. does not disclose at least one miniature clock buffer, wherein said at least one miniature clock buffer is a scaled version of said clock buffer, said miniature clock buffer having a scaling factor of K, said scaling factor representing a number of said miniature clock buffers utilized to minimize negative variations experienced by said clock buffer.

However Masleid et al. discloses at least one miniature clock buffer, wherein said at least one miniature clock buffer is a scaled version of said clock buffer, said miniature clock buffer having a scaling factor of K, said scaling factor representing a number of said miniature clock buffers utilized to minimize negative variations experienced by said clock buffer (col. 2, lines 52-66, col. 5, lines 14-26).

Art Unit: 2634

Therefore it would have been obvious to one or ordinary skill in the art to modify Fong et al. in view of Masleid et al. to incorporate at least one miniature clock buffer, wherein said at least one miniature clock buffer is a scaled version of said clock buffer, said miniature clock buffer having a scaling factor of K, said scaling factor representing a number of said miniature clock buffers utilized to minimize negative variations experienced by said clock buffer in order to have a strong skewed distribution of power consumption and provide minimum clock latency (Masleid et al., col. 2, lines 55-56, 64-65).

- (2) With regard to claim 2, claim 2 inherits all the limitations of claim 1. Masleid et al. further discloses driving of said received clock signal is performed by adding a gain factor to said received clock signal, thereby increasing strength of said clock signal to allow propagation to said register (col. 1, lines 20-28, col. 2, lines 52-66, col. 5, lines 14-19, 61-64).
- (3) With regard to claim 3, claim 3 inherits all the limitations of claim 1. Masleid et al. further discloses wherein said clock buffer provides an amount of delay that slows progression of said clock signal in a path to said register (col. 1, lines 59-63, col. 2, lines 52-66).
- 6. Claims 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fong et al. (US Patent Application 2002/0154718), in view of Masleid et al. (US Patent 6,532,544) as applied to claim 1, in view of Liepe (US Patent 6,788,754).

(1) With regard to claim 4, claim 4 inherits all the limitations of claim 1. Fong et al. in combination with Masleid et al. disclose all the limitations of claim 1 above. However Fong et al. in combination with Masleid et al. do not disclose wherein said negative variations are selected from the group consisting of process, voltage and temperature.

However Liepe discloses in wherein said negative variations are selected from the group consisting of process, voltage and temperature (col. 1, lines 13-21, 41-48, 52-56, col. 2, lines 60-63, col. 3, lines 44-46, col. 8, lines 5-9).

Therefore it would have been obvious to one of ordinary skill in the art to modify Fong et al. in combination with Masleid et al. in view of Liepe to incorporate wherein said negative variations are selected from a group consisting of process, voltage and temperature in order to achieve transmission time consistency among a plurality of signal paths (Liepe, col. 1, lines 49-51).

(2) With regard to claim 5, claim 5 inherits all the limitations of claim 1. Liepe further discloses wherein said system is located within receive logic situated on an application specific integrated circuit because they have undesired transmission time variations between alternative signal paths (col. 1, lines 7-11, col. 2, lines 50-54).

Allowable Subject Matter

7. Claims 6 and 7 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The following is a statement of reasons for the indication of allowable subject matter: The instant application discloses a system for

Art Unit: 2634

matching data and clock signal delays. Prior art references show similar methods but fail to teach: "a setup time of said receive logic is represented by the equation:

T.sub.setup=T.sub.reg-setup+0.1.times.(-T.su-b.clk-dly)-T.sub.clk-rte(min)

wherein, T.sub.reg-setup is a setup time for said register, T.sub.clk-dly is a delay contributed by said clock buffer, and T.sub.clk-rte(min) is a minimum delay contributed by propagation of said clock signal to said register", as in claim 6; and "in a hold time of said receive logic is represented by the equation:

T.sub.hold=T.sub.reg-hold+0.1.times.(T.sub.c-lk-dly)+T.sub.clk-rte(max) wherein,
T.sub.reg-hold is a hold time for said register, T.sub.clk-dly) is a delay contributed by said clock buffer, and T.sub.clk-rte(max) is a maximum delay contributed by propagation of said clock signal to said register", as in claim 7.

- 8. Claims 8-20 are allowed.
- 9. The following is a statement of reasons for the indication of allowable subject matter: The instant application discloses a system for matching data and clock signal delays. Prior art references show similar methods but fail to teach: "minimizing set up and hold times of said receive logic", as in claims 8, 15.

Conclusion

- 10. The prior art made record of and not relied upon is considered pertinent to applicant's disclosure:
- a. Kim, US Patent 6,424,190 discloses an apparatus and method for delay matching of full and divided clock signals.

Art Unit: 2634

b. Coddington et al. US Patent 6,294,938 discloses a system with DLL.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cicely Ware whose telephone number is 571-272-3047. The examiner can normally be reached on Monday – Friday, 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on 571-272-3056. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9314 for regular communications and 703-872-9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Cicely Ware

cqw April 5, 2005 AMANDAT. LE
PRIMARY EXAMINER